Laboratoire Architectures Intégrées Radiofréquences

Internship Proposal 2024
Robust System Optimization for better energy efficiency in Advanced Silicon Systems

For any information, questions, discussions, help please feel free to contact dominique.morche@cea.fr, pierre.courouve@cea.fr
+33 4 38785403
Research Director in LAIR laboratory

Sujet de stage :

Contexte

Ce projet s'inscrit dans le cadre d'une longue et fructueuse collaboration entre le CEA (Grenoble) et Ampère-lab (Lyon) visant à développer des méthodes de conception efficaces pour les systèmes de radiofréquence, basées sur une approche de contrôle et de système. Ampère-lab est une unité mixte de recherche (CNRS, Ecole Centrale de Lyon, INSA Lyon, Université Lyon 1) de plus de 150 chercheurs basée à Lyon, France, qui travaille sur l'utilisation rationnelle de l'énergie dans les systèmes en relation avec leur environnement. Ses recherches portent notamment sur l'analyse, le contrôle et la conception de systèmes complexes basés sur l'optimisation.

Background Scientifique:

Depuis la prise de position récente de l'UE sur la souveraineté en matière de silicium, l'importance de la maîtrise des technologies de conception de circuits intégrés est apparue stratégique. Cependant, cette conception devient de plus en plus complexe à mesure que la technologie évolue (la technologie 5nm est actuellement en cours d'industrialisation et la technologie 3nm est la prochaine génération). En particulier, la variabilité des paramètres des transistors augmente considérablement (voir la figure 1). De plus, la nécessité de réduire la consommation d'énergie est cruciale pour un système autonome (voir Fig.2) et deviendra obligatoire dans tous les systèmes futurs. Par conséquent, l'optimisation des systèmes devient de plus en plus importante. De nouvelles approches d'optimisation sont nécessaires pour améliorer l'efficacité énergétique des systèmes et mieux tirer parti des technologies du silicium. Jusqu'à présent, l'optimisation par programmation géométrique (sous-classe de l'optimisation convexe), implémentée dans CVX, est utilisée par les chercheurs du CEA pour améliorer les méthodologies de conception. Cependant, l'utilisation de cette technique d'optimisation particulière impose de fortes contraintes sur la simplicité du modèle mathématique utilisé.

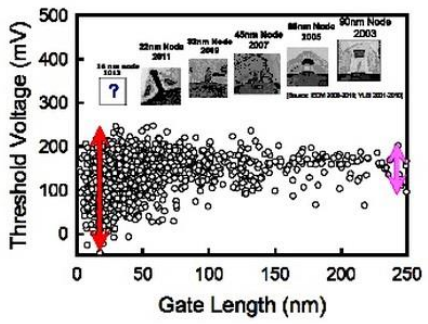


Fig 1. Variations de la tension de seuil en fonction de la longueur de la grille, montrant l'augmentation de la plage avec la reduction de la longueur de grille

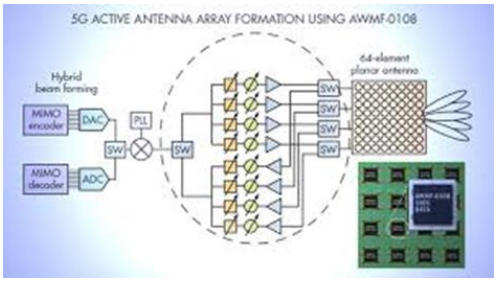


Fig 2. System Hétérogene pour communications 5G

Dans le cadre du stage, l'objectif sera d'explorer la méthodologie d'optimisation pour le cas d'utilisation d'un filtre analogique décrit dans la Fig.3. Ce bloc est embarqué dans tous les systèmes de communication (WiFi, BTLE, Lora, UWB, ...) mais aussi dans toutes les interfaces de capteurs. L'optimisation de sa puissance vis à vis des contraintes de bruit, de linéarité et de bande passante est donc un enjeu majeur.
L'objectif de la mission est donc d'évaluer la possibilité de mettre en place une nouvelle approche Contrôle et Système basée sur l'Optimisation Convexe pour améliorer la méthodologie de conception des circuits analogiques.

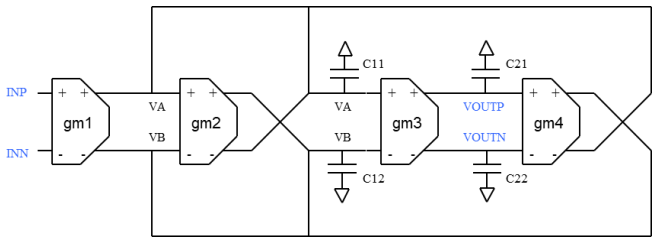


Fig 3 . Architecture of gmC filter used for wireless communication

Déroulement de la Mission (proposition)

1. Le candidat retenu se familiarisera d'abord avec le problème de conception d'un point de vue théorique et pratique. Un accent particulier sera mis sur la relation entre la performance du filtre (consommation, linéarité, bruit, …) et la performance des building blocks et des cellules élémentaires (transistors), en utilisant des modèles de complexité différente. Les résultats seront validés grâce à des simulations électriques (2 mois).
2. Il/elle fera ensuite une revue (avantages/limites) des méthodes actuelles de conception des filtres gmC basées sur la simulation (SPICE) en travaillant avec des concepteurs d'expériences. Une figure de mérite sera établie afin de pouvoir évaluer la qualité de la conception (2 mois).
3. Il/elle proposera une nouvelle méthode de conception basée sur l'optimisation de la programmation géométrique pour surmonter ces limitations. En particulier, l'idée est d'obtenir une formulation mathématique du problème de conception basée sur une approche systémique, et éventuellement sur des techniques de relaxation convexe, sera étudiée (un mois).
4. La tâche finale consistera à rédiger le rapport de stage et à envisager une publication potentielle dans une conférence internationale (un mois).

Durée : 6-mois de stage démarrant entre Février et Avril 2024
Localisation: CEA, Grenoble
Profil:

- Etudiants en 2ème ou 3ème année d'école d'ingénieur ou étudiants en Master 1 ou 2 intéressés par la théorie du contrôle et des systèmes, l'optimisation et les mathématiques appliquées.
- Des connaissances supplémentaires en microélectronique, en conception de systèmes RF ou en optimisation convexe seraient un plus.
- Motivation et capacité à travailler au sein d'une équipe de recherche dans un environnement multidisciplinaire qui favorise l'équilibre entre les activités académiques et industrielles.
- Bonne capacité de rédaction et de communication en anglais.

Perspectives:

Ce travail sera le point de départ d'une thèse de doctorat qui débutera à l'automne 2024. Le stagiaire sélectionné sera un candidat naturel pour cette thèse, s'il le souhaite.

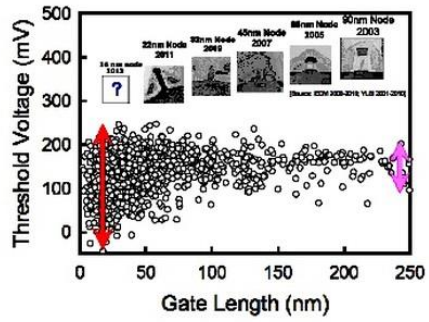
Internship Topic

Context

This project is part of the longstanding and fruitful collaboration between CEA (Grenoble) and Ampère-lab (Lyon) to develop efficient design methods for RadioFrequency systems based on a Control and System approach. Ampère-lab is a joint research unit (CNRS, Ecole Centrale de Lyon, INSA Lyon, Université Lyon 1) of over 150 researchers based in Lyon, France, working on the rational use of energy in systems in relation to their environment. In particular, its research focuses on the analysis, control and design of complex systems based on optimization.

Scientific Background:

Since the recent strategic position of EU on the targeted silicon sovereignty, the importance of mastering silicon technologies has become clear. However, with the technology scales (5nm technology is currently being industrialized and 3nm is the next generation) the design becomes more and more complex. In particular, the variability of the transistor parameters is dramatically increasing, see Fig. 1. Moreover, the necessity to reduce the power consumption is crucial for an autonomous system (see Fig.2) and become mandatory in all future systems. As a result, system optimization is becoming more and more important. New optimization approaches are needed to improve system energy efficiency and to better take benefit of the silicon technologies. Up to now, Geometric Programming Optimization (sub-class of convex optimization), implemented in CVX, is used by CEA researchers to improve design methodologies. However, the use of this particular optimization technique imposes strong constraints on the simplicity of the mathematical model used.



Courtesy of Prof. Yiming Li, National Chiao Tung University, Taiwan

Fig 1. Simulation of threshold voltage variations vs gate length, showing the increasing range as devices are

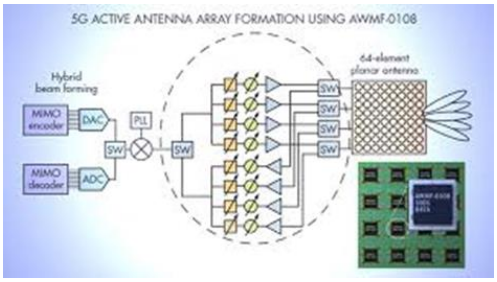


Fig 2. Heterogeneous System for 5G communications

Mission Objective

In the context of the internship, the objective will be to explore the optimization methodology to the use case of an analog filter depicted in Fig.3. This block is embedded in all communication system (WiFi, BTLE, Lora, UWB, …) but also in all sensor interfaces. Its power optimization versus linearity, noise and bandwidth is therefore a key challenge.

The mission objective is therefore to evaluate the possibility to setup a new Control and System approach based on Convex Optimization to improve the design methodology of analog circuits.

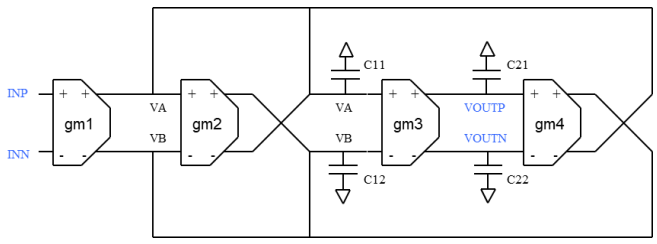


Fig 3 . Architecture of gmC filter used for wireless communication

Mission schedule (proposition)

1. The successful candidate will first familiarize himself/herself with the design problem from both a theoretical and a practical point of view. Particular emphasis will be placed on relating the filter

performance (power consumption, gain, cut-off frequency…) to the characteristics of the building blocks (transistors), using models of different complexity. The results will be validated thanks to electrical simulations (2 months).

2. He/She will then make a review (advantages/limitations) on current design methods for gmC filters based on simulation (SPICE) by working with some experiment designers. Figure of Merit will be establish in order to be able to evaluate the quality of the design (2 months).
3. He/She will propose a new design method based on geometric programming optimization to overcome these limitations. In particular, the idea is to obtain the mathematical formulation of the design problem based on a System approach, and possibly on convex relaxation techniques, will be investigated (one month).
4. The final task will be to write the internship report and to consider a potential publication in some international conference (one month).

Duration : 6-months internship starting between February and April 2024
Location: CEA, Grenoble
Profile:

- Students of 2nd or 3rd year in Engineering School or Master 1 or 2 students interested in **Control and System theory**, **Optimization** and **Applied Mathematics**.
- Additional knowledge in **Microelectronics**, **RF system design** or **Convex optimization** would be a plus.
- **Motivation** and **ability** to work as part of a research team in a multidisciplinary environment that promotes a balance between academic and industrial activities
- Good writing and communication skills in English.

Perspectives:

This work will be the starting point of a PhD thesis that will begin in fall 2024. The selected trainee will be a natural candidate for this thesis, if he/she so wishes.

Working Environnement

Introducing Leti: a key player in innovation

As a laboratory of the CEA (French Atomic Energy Commission), LETI (Electronics and Information Technology Laboratory) is today one of the most important R&D laboratories in Europe in the field of electronics, microelectronics and more generally microtechnologies. LETI has developed around two main activities: future technologies for the semiconductor industry, and the design of advanced electronic systems. Its vocation is to help industrialists to increase their competitiveness through technical innovation and the transfer of its technological know-how. More than 85% of its activity is devoted to finalized research with more than 200 industrial partners and 350 contracts per year. Léti has created nearly 30 high-tech start-ups, including Soitec, the world leader in silicon-on-insulator. It files some 180 patents per year and manages a portfolio of 2,800 patents that helps strengthen the competitiveness of its industrial partners. With more than 250 students involved in research activities, Leti is a source of skills dedicated to innovation.

Minatec Center in CEA-Leti Grenoble

Grenoble an exceptional environment

Technologies that have become products

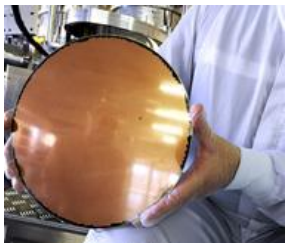
Weighing sensors from Terraillon, shock sensors for airbags from Freescale, night vision detectors, imagers for Nokia cell phone cameras, low-power processors from STMicroelectronics, a rapid avian flu virus analyzer, a digital X-ray image sensor, etc. are all examples of Leti technologies that have become commercial products.

Start-ups become world leaders

With a strong business creation activity, Leti is one of the most prolific research institutes in the world in terms of technological start-ups: SOITEC, SOFRADIR, ULIS, MOVEA, APIX Technology, HELIODEL... and others to come...

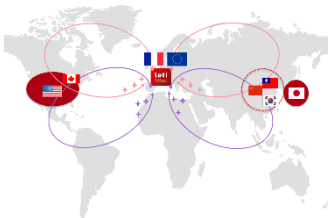
World-class research infrastructures

For research that is as close as possible to industrial requirements, Leti has consolidated rare technological resources: a nano-characterization platform, 300mm and 200mm lines dedicated to nano-electronics and MEMS, a 3D integration line, in 8,000 square meters of clean rooms



A major player in France with a worldwide footprint

Along with 32 other research institutes, Leti is part of the Carnot Institute network, which is strongly committed to helping industry foster innovation and economic dynamism.
Leti has developed close international partnerships, forming the Hi-Tech Alliance with Fraunhofer (GE), CSEM (CH) and VTT (FI), creating the NanoVLSI Alliance with Caltech, partnering with IBM and ST on



nanoelectronics, and joining the industrial consortium on microsystems (MMC) in Japan

Leti, Cea Tech's technology research institute, is dedicated to innovation and transferring innovation to industry. Its core business is microelectronics, component miniaturization, system integration and integrated circuit architecture technologies, which are the basis for the Internet of Things, artificial intelligence, augmented reality and connected health. The institute is located in Grenoble with two offices in the USA and Japan, and has 1800 researchers.
The PhD will take place at LETI, in the Radio Frequency Integrated Architectures laboratory belonging to the wireless technologies department. The laboratory develops multi-technology integrated systems of the System-In-Package (SiP) and System-On-Chip (SoC) type and advanced integrated circuits of very high complexity for industrial partners as well as for large groups, SMEs and start-ups. The LAIR laboratory develops innovative solutions for various applications such as consumer, telecom, aeronautics, automotive, environmental monitoring, and health. More specifically, the LAIR laboratory develops integrated radio frequency systems covering a wide spectrum of applications such as RFID, UWB, PMR, mmW, 6G, iOT, sensing and monitoring...

Presentation of the Integrated Radiofrequency Architectures laboratory

The Radio Frequency Integrated Architectures laboratory (LAIR) belongs to the Wireless Technologies Department of LETI. It develops multi-technology integrated systems of the System-In-Package (SiP) and System-On-Chip (SoC) type and advanced integrated circuits of very high complexity for industrial partners in various fields (telecommunications, health), as well as for large groups, SMEs and start-ups.

In 5G and its future evolution (6G), satellite communications and Industry 4.0, the major challenges for wireless communication systems are to integrate the necessary functions into the most compact and energy-efficient systems possible. In addition, the increase in throughput and communication range requires the use of increasingly high transmission power and frequency bands, with increasingly wide bandwidths. Also, as systems become more complex, it becomes necessary to combine different technologies and to integrate the mixed dimension or digital with analog/RF functions in order to achieve optimal system performance.

The laboratory develops competences in the fields of RF and millimeter wave (mmW), internet of things (IOT), and utra wide band (UWB). The applications of SiPs and SoCs concern wireless communication in many fields:

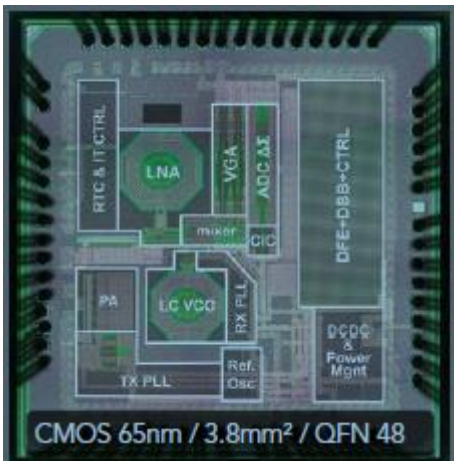
- Very high speed communication at millimeter frequencies over short distances
- Telecommunication in the 5G bands
- Communication with space in low orbit
- Localization inside buildings with an accuracy of 1 cm
- Communication with Sigfox networks
- Radar for health, monitoring of physiological parameters of a person or generation of endorphins through waves
- Sensing of the environment

The candidate will benefit from an integration within the team where he/she will fully participate in the life of the laboratory. He/she will benefit from all the tools of the System-on-Chip design flow set up in the last few years, including high level (Matlab/Simulink) and low level (Cadence/Eldo/Spectre/ADMS) design tools. As a laboratory hosting PhD and trainee (10 students per year), the LAIR fully integrates its students in the various activities of a research laboratory, and in particular in the production of scientific articles.

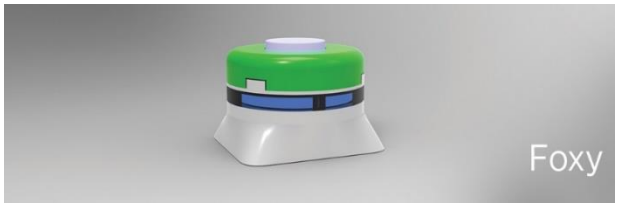
Examples of demonstrators realized in the Integrated Radiofrequency Architectures laboratory

- Foxy Circuit

Domain : IoT



Puce Foxy en technologie CMOS 65 nm



Foxy integrates, on a single chip, a sub-1 GHz RF transceiver used to connect objects to the Sigfox network worldwide.

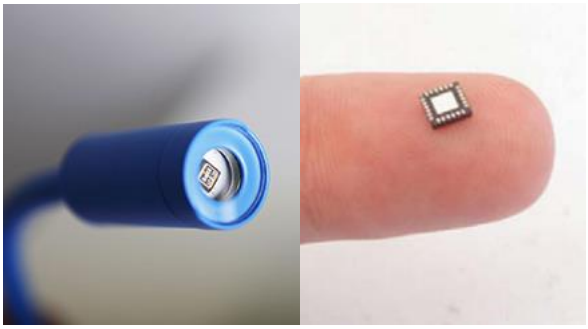
This chip uses Ultra Narrow Band (UNB) technology and optimizes the network capacity while maximizing the transmission budget for Low-Power Wide-Area (LPWA) communication networks.

Foxy is the first wireless transceiver specifically dedicated to UNB technology. Built in 65 nm CMOS technology, it allows to realize GFSK and DBPSK modulations and to reach data rates from 100 bps to 20 kbps.

- Circuit G-Link

Domain : mmW

Application : high speed short range transmission



Puce G-link en technologie CMOS 65 nm

G-Link is a low-power 60 GHz wireless connection that allows for the instant transfer of several gigabits of data between two devices separated by a few centimeters.

This circuit allows sharing HD video, between a camera and a video screen, between a kiosk and a tablet to download HD video, etc.

This is a secure application in industrial environments where cable reliability is a major concern in terms of data transfer. For example, any device in which the connectors are subject to rotation, vibration or pressure that reduces their life span can be replaced by G-Link.